REMARKS

I. Introduction

In response to the pending rejection, the Applicants have amended claims 1, 2, 7 and 8 so as to more specifically define the subject matter of the present invention, as well as to address the rejection of the claims under 35 U.S.C. § 112, second paragraph. Support for the subject matter added to claims 1 and 7 can be found, for example, in Fig. 1, and the corresponding description of the specification.

With regard to the rejection of the claims under 35 U.S.C. § 112, second paragraph, the claim language that formed the basis of the rejection has been deleted from the claims, and therefore it is submitted that the rejection has been overcome.

For the reasons set forth below, it is respectfully submitted that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 103

Claims 1, 3, 5 and 7 were rejected under 35 U.S.C. § 103 as being unpatentable over USP No. 5,701,308 to Attaway in view of USP No. 6,671,847 to Chao. Applicants respectfully submit that, as amended, the foregoing claims are patentable over Attaway and Chao, taken alone or in combination with one another.

The present invention relates to a path delay measuring circuit which can automatically measure the path delay in a combination circuit without requiring the use of an LSI tester. One of the benefits of the present invention is the simplicity of the design of the circuit. As recited by the amended claims, each of the first, second and third flip-flops contained in the path delay measuring circuit are clocked utilizing the same clock signal. For example, referring to Fig. 1,

the clock input of each of the first, second and third flip-flop receive the same clock signal output by the timing signal creating circuit.

Turning to the cited prior art, in Attaway, the internal scan register (which is relied on as corresponding to the first flip-flop) and the boundary scan register (which is relied on as corresponding to the second flip-flop) receive different clock signals, CLK and TCK, and the third flip-flop of Attaway is not even illustrated in the figures, so it is not clear which clock signal the third flip-flop of Attaway receives. As such, at a minimum, Attaway fails to disclose the circuit recited by the amended claims which includes the first, second and third flip-flop all being clocked by the same clock signal, and in fact teaches away from the recited circuitry. Furthermore, Chao does not cure this deficiency of Attaway and is not relied upon as doing so in the pending rejection.

Accordingly, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a *prima facie* case of obviousness (*see*, M.P.E.P. § 2143.03), and for at least the foregoing reasons the combination of Attaway and Chao fails to do so, claims 1, 3, 5 and 7 are patentable over Attaway and Chao taken alone or in combination.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 1 and 7 are patentable for the reasons set forth above, it is respectfully submitted that all other dependent claims are also in condition for allowance.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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